This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A circuit for correlating an input signal comprising:
a parallel array of processing elements, each of said processing elements comprising an ~~a series of~~ analog sampling circuit ~~unit processing elements, each analog sampling unit processing element comprising a sample and hold device~~ for sampling the input signal in response to a timing signal, and a circuit for scaling the resulting sample according to a predetermined scaling factor;
a timing circuit for causing said timing signal to be presented in time-delayed succession to successive ones of said analog sampling unit processing elements, said timing circuit comprising a timing element in parallel with an associated analog sampling unit processing element, and said timing element comprising a phase lock loop or a delay lock loop; and,
means for multiplying the output of each analog sample unit processing element to scale the output and summing the scaled outputs of said processing elements.

2. (Originally Presented) A circuit as in claim 1 wherein the scaling factors in successive processing elements correspond to the coefficients in a Fourier series approximation of a desired frequency response.

3. (Originally Presented) A circuit as in claim 1 wherein said timing circuit comprises a plurality of delay elements, the outputs of which are presented to successive ones of said processing elements.

4. (Originally Presented) A circuit as in claim 1 wherein said circuit for scaling comprises a multiplier having as inputs the output of said sampling circuit and a predetermined scaling factor, the outputs of said multipliers being summed.

5. (Originally Presented) A circuit as in claim 1 wherein the scaling factors in successive processing elements correspond to the coefficients in a Fourier series approximation of a desired frequency response, said timing circuit comprises a plurality of delay elements, the outputs of which are presented to successive ones of said processing elements, and said circuit for scaling comprises a multiplier having as inputs the output of said sampling circuit and a predetermined scaling factor, the outputs of said multipliers being summed.

6. – 9. (Canceled)

10. (Currently Amended) A circuit for correlating an input signal with a desired frequency response, comprising:

a first and a second arrays of parallel processing elements, each of said processing elements comprising an ~~a series of~~ analog sampling circuit ~~unit processing elements, each comprising a sample and hold device~~ for sampling the input signal in response to a timing signal, and a multiplier circuit for scaling the resulting sample according to a predetermined scaling factor;

a timing circuit for causing said timing signal to be presented in time-delayed succession to successive parallel pairs of said analog sampling unit processing elements, said timing circuit comprising a timing element in parallel with an associated analog sampling unit processing element, and said timing element comprising a phase lock loop or a delay lock loop;

a summer for summing the scaled output of said processing elements comprising said first array; and,

a summer for summing the scaled output of said processing elements comprising said second array.

11. (Originally Presented) A circuit as in claim 10 wherein the scaling factors in successive processing elements of said first array correspond to the coefficients of a Fourier series approximation of the normal component of said desired frequency response

and the scaling factors in successive processing elements of said second array correspond to the coefficients of a Fourier series approximation of the quadrature component of said desired frequency response.

12. (Originally Presented) A circuit as in claim 10 wherein said first array represents a normal channel and said second array represent a quadrature channel.

13. (Previously Amended) A circuit as in claim 10 wherein said timing circuit comprises a plurality of delay elements in series, the outputs of which are presented to successive ones of said processing elements in sequence.

14. (Previously amended) The method of correlating an input signal to an apparent reference signal, comprising:

providing phase shifted timing signals to a plurality of analog sample and hold circuits to generate a series of phase shifted analog samples of the input signal;

multiplying successive ones of said samples by coefficient values representing the normal component of said reference signal to scale said samples;

multiplying successive ones of said samples by coefficient values representing the quadrature component of said reference signal to scale said samples;

summing said normal scaled samples;

summing said quadrature scaled samples; and,

deriving the root mean square of said normal and quadrature sums.

15. (Canceled)

16. (Originally Presented) The method of claim 14 wherein said coefficient values comprise the coefficients of a Fourier series approximation of the frequency response of said reference signal.

17. (Previously Amended) A circuit as in claim 1 wherein said scaling factors are adjusted to alternate between scaling factors representing alternately a normal and a quadrature channel sets of coefficients of a Fourier series approximation of a desired frequency response.

18. – 19. (Cancelled)

20. (Previously amended) The circuit of claim 1 for correlating an input signal with an apparent reference signal wherein the apparent reference signal is embedded in an array of analog sampling circuits by means of scaling factors representative of the characteristics of said reference signal, and wherein the sampling point for the input signal advances through successive sampling circuits.